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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

TRAN, MICHAEL THANH

ART UNIT PAPER NUMBER

2827

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

10/749,690

Applicant(s)

HALBERT ET AL.

Examiner

Michael t. Tran

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on December 30, 2003 through June 24, 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-6 and 16-22 is/are allowed.
- 6) ☒ Claim(s) 7 and 12 is/are rejected.
- 7) ☒ Claim(s) 8-11 and 13-15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

- 5) ☐ Notice of Informal Patent Application (PTO-152)

- 6) ☐ Other: _____.

MICHAEL TRAN

PATENT EXAMINER

DETAILED ACTION

1. In response to the Communications dated December 30, 2003 through June 24, 2004, claims 1-22 are active in this application.

Claim Objections

2. Claims 8-11 and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claim 7 is rejected under 35 U.S.C 102(b) as being anticipated by Barth et al. [U.S. Patent RE37,409 E].

With respect to claim 7, Barth et al. disclose a controlling device comprising: a first storage location [117 of figure 3] in which data concerning the status of both rows of memory cells [figure 3] and rows of sense amplifiers [350 of figure 3] within a bank of memory cells within a memory device is stored; control logic [118 of figure 3] coupled to the first storage location to check data within the first storage location to determine if the contents of a specific row of sense amplifiers is dirty [see columns 4 and 1st paragraph of column 5]; and a memory bus [see interconnections between 117 and 118 of figure 3; also see column 4] coupling to the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device.

5. Claim 12 is rejected under 35 U.S.C 102(b) as being anticipated by Barth et al. [U.S. Patent RE37,409 E].

With respect to claim 12, Barth et al. disclose a computer system comprising: a processor [see 2nd paragraph of column 4]; a memory device having at least one bank [see figure 3] in which a plurality of memory cells are organized into rows; a memory controller [118 of figure 3] coupled to the processor and having a first storage location that the memory controller accesses to determine if the contents of a specific row to which data is to be written in response to a request from the processor to write data is already cached by a specific row of sense amplifiers, to check if the specific row is the

open row within the bank, and to check if the data cached by the specific row of sense amplifiers is dirty [see columns 4 and 5]; and a memory bus [see interconnections between 114, 117, and 118 of figure 3] coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device.

Allowable Subject Matter

6. Claims 1-6 and 16-22 are allowable over the prior art of record.
7. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:
 - Isolator control logic to coordinate the operation of the first set of common isolators to allow data received from outside the memory device and present on the plurality of global I/O lines to be latched by the first row of sense amplifiers, to store an indication that the data latched by the first row of sense amplifiers is dirty, to coordinate the operation of the first set of subarray isolators to allow data latched by the first row of sense amplifiers to be written back to a row of memory cells within the first subarray, and to remove an indication that the data latched by the first row of sense amplifiers is dirty.
 - Transmitting a mini write command to the memory device to write the data transmitted to the memory device to at least a portion of the specific row of sense amplifiers if the contents of the specific row of memory cells have been copied to

the specific row of sense amplifiers, the specific row of memory cells is the open row of the bank of the memory device.

- Operating a second set of isolators coupled between a first set of bit lines and the first row of sense amplifiers in response to the receipt of a writeback command to allow the data latched by the first row of sense amplifier to be copied to and stored in a first row of memory cells also coupled to the first set of bit lines.
- Program a memory controller to transmit a mini write command to write data to the row of sense amplifiers and store an indication that the data latched in the row of sense amplifiers is dirty in lieu of writing the data to the row of memory cells being cached by the row of sense amplifiers.

Conclusion

8. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

10. Any inquiry of a general nature or relating to the status of this application

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should be directed to the Group receptionist whose telephone number is (571) 272-1650.



Michael T. Tran

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March 9, 2005

MICHAEL TRAN
PRIMARY EXAMINER